Inver Hills Community College

ENGR 2043: Introduction to Digital Circuits and Logic Design

A. COURSE DESCRIPTION

Credits: 4

Lecture Hours/Week: 3

Lab Hours/Week: 2

OJT Hours/Week: *.*

Prerequisites:
This course requires the following prerequisite
ENGR 2041 - Linear Circuits I (Minimum grade: 1.67 GPA Equivalent)

Corequisites: None

MnTC Goals: None

Provides an introduction to digital logic and logic design. Topics include binary systems, logic gates, Boolean algebra and functions, Karnaugh map, design of combinational and sequential logic circuits, adders, decoders, multiplexers, comparator counters, registers and memories. Students cannot receive credit for both ENGR 1060 and ENGR 2043. Prerequisites: A grade of C or higher in ENGR 2041, or consent of instructor.

B. COURSE EFFECTIVE DATES: 08/26/2013 - Present

C. OUTLINE OF MAJOR CONTENT AREAS

1. Binary, Octal, and Hexadecimal systems (5%)
2. Boolean Algebra (15%)
3. Karnaugh Maps (10%)
4. Combinational Circuit Design & Simulation (10%)
5. Multiplexers, Decoders and Programmable Logic Devices (10%)
6. Latches, Flip Flops, Registers and Counters, Serial Adders (15%)
7. Clocked Sequential Circuits (10%)
8. State Tables and Graphs (10%)
9. Sequential Circuit Design (10%)
10. Introduction to VHDL (5%)

D. LEARNING OUTCOMES (General)

1. Demonstrate conversion of numbers to/from binary, octal, decimal & hexadecimal systems and use binary coding schemes.
2. Solve and/or simplify Boolean functions by algebraic and mapping methods.
3. Construct logic circuits with logic gates to represent Boolean functions.
4. Identify the characteristics and truth tables for integrated circuits such as logic gates, flip-flops, multiplexers, counters and registers.
5. Design, analyze, and simulate/test a combinational logic circuit on the level of difficulty of a decimal to binary encoder or full adder-subtractor.
6. Design, analyze, and simulate/test a sequential logic circuit on the level of difficulty of a BCD counter or serial adder-subtractor.
7. Identify equivalent Boolean representation corresponding to an elementary VHDL code.

E. Minnesota Transfer Curriculum Goal Area(s) and Competencies

None

F. LEARNER OUTCOMES ASSESSMENT

As noted on course syllabus

G. SPECIAL INFORMATION

None noted